

**Digital Logic Lab Assignment # 8**

* To verify the operation of Half Subtractor Circuit
* To verify the operation of Full Subtractor Circuit

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**OBJECTIVE 8.1:**

**TO VERIFY THE OPERATION OF HALF SUBTRACTOR CIRCUIT.**

**THEORY:**

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

**Boolean Expressions:**

HS (D) = AB’+A’B

HS (B) = A’B

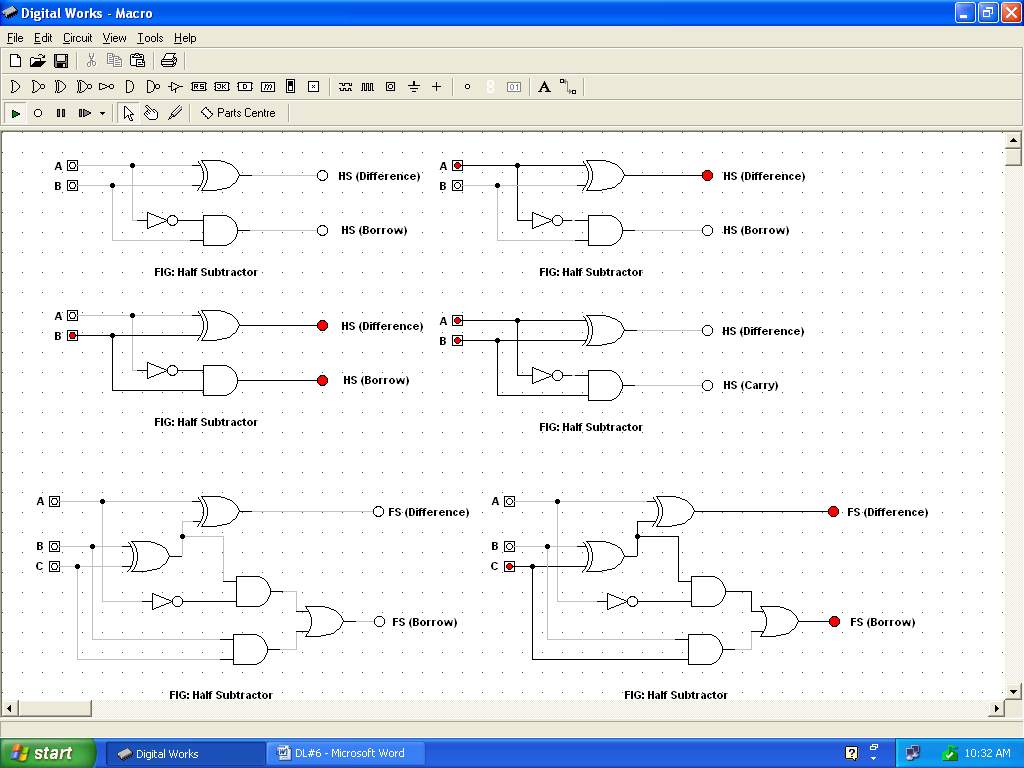
**BLOCK DIAGRAM:**

Half Subtractor

**A Borrow**

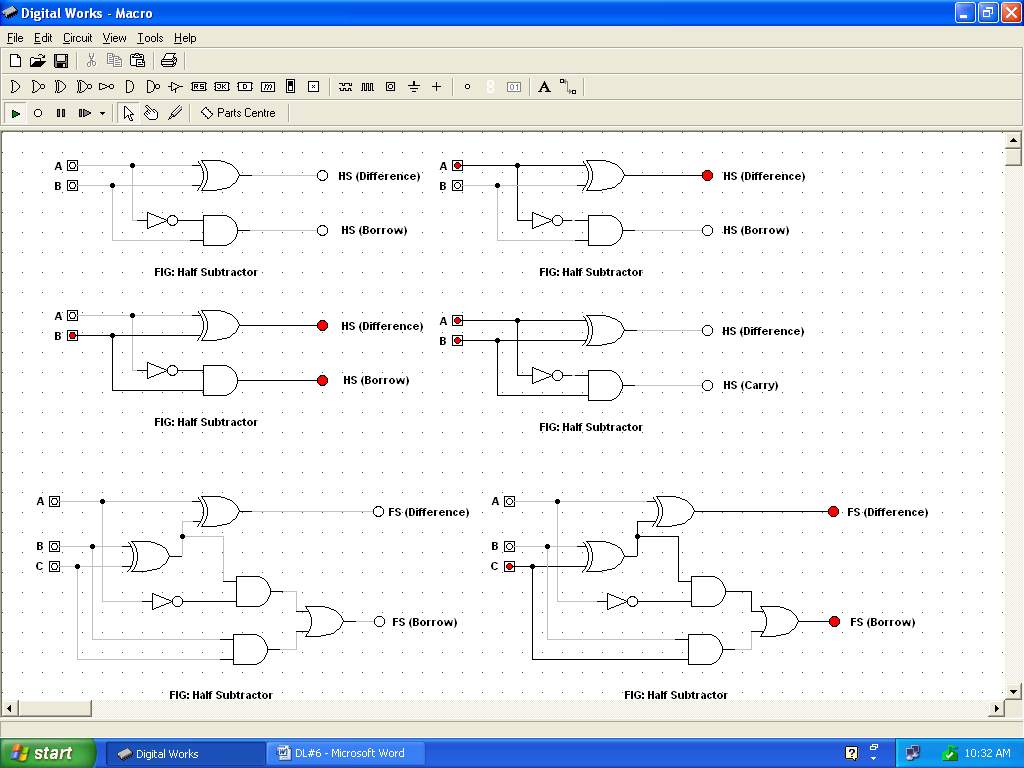
**B Difference**

**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **BORROW** | **DIFFERENCE** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

**OBSERVATIONS:**

**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **BORROW** | **DIFFERENCE** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

**CONCLUSION:**

Hence, operation of Half Subtractor is verified.

**REFERENCE:**

M. Morris Mano (Digital Logic and Computer Design)

**OBJECTIVE 8.2:**

**TO VERIFY THE OPERATION OF FULL SUBTRACTOR CIRCUIT.**

**THEORY:**

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, X (minuend) and Y(subtrahend) and Z (subtrahend) and two outputs D (difference) and B (borrow).

**Boolean Expressions:**

HS (D) = A’B’C+A’BC’+AB’C’+ABC

HS (B) = A’B’C+A’BC’+A’BC+ABC

**Block Diagram:**

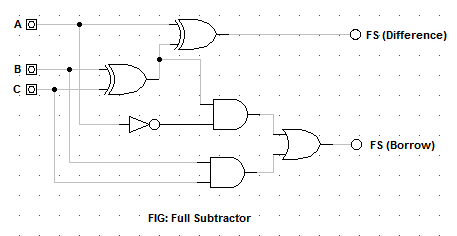
**A Borrow**

Full Subtractor

**B**

**C Difference**

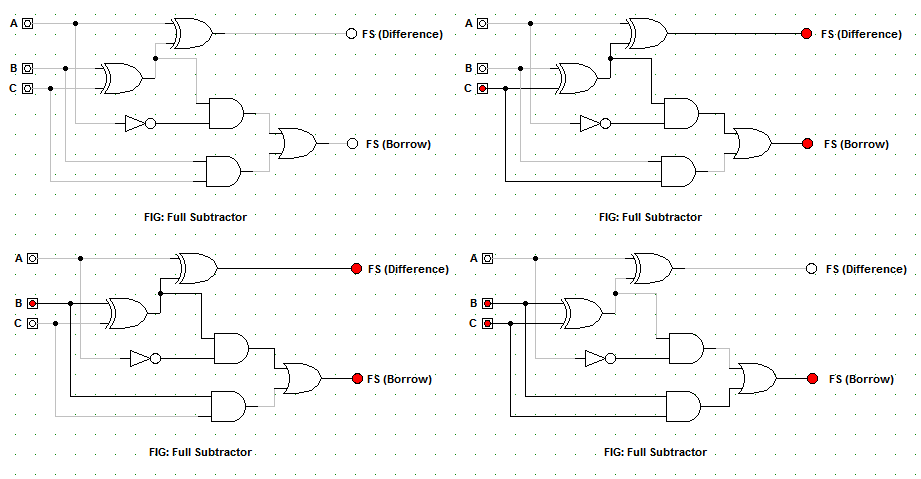
**CIRCUIT DIAGRAM:**

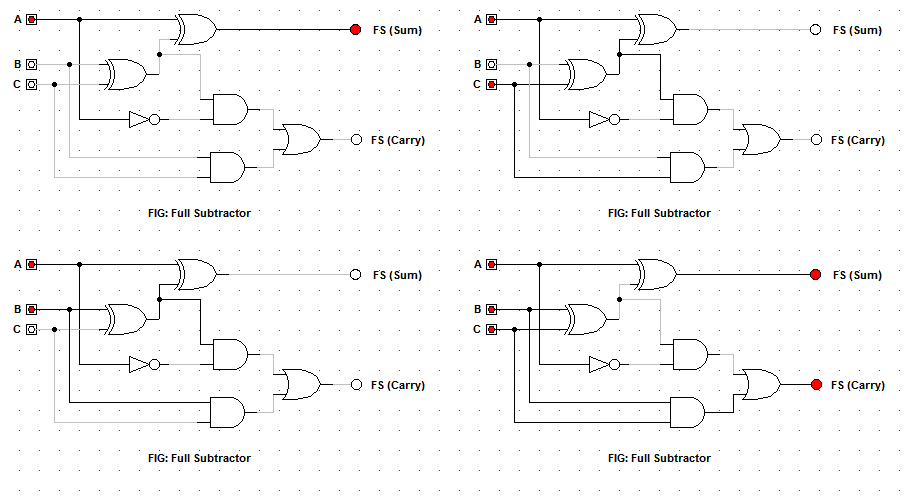
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**TRUTH TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **BORROW** | **DIFFERENCE** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**OBSERVATIONS:**

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**OBSERVATION TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **BORROW** | **DIFFERENCE** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**CONCLUSION:**

Hence, operation of Full Subtractor is verified.

**REFERENCE:**

M. Morris Mano (Digital Logic and Computer Design)